(Affiliated to University of Mumbai)	***End Semester Examination (R-24) SH 2025 Answer Key with marking scheme***
Branch: CSE(IoT&CSIBCT)	Course: Computer Organization and Architecture
Year/ Semester:SE/III	Course code: CSEC305
Time: 02 hours	Marks: 60

		Marks
Q. 1	Attempt any FOUR. (All questions carry equal marks)	
A.	Differentiate between Computer organization and Computer Architecture. Any 5-8 valid points-5 M	05
B.	Represent (1449.125)10 using double precision format of IEEE 754 standards. 0x4096A48000000000	05
C.	Explain various addressing modes of 8086. 5 types-5 M	05
D.	Explain the concept of locality of reference.	05
Q.2	Attempt any FOUR. (All questions carry equal marks)	
A.	Differentiate between a Von-Neumann and Harvard architecture. Explain concept of a microprogrammed control unit and compare it with a hardwired control unit. 5-8 valid points-5 Marks Each	10
B.	Analyze the concepts of Segmentation and Paging in virtual memory. Explain the Address Translation Mechanism for a paged virtual memory system. Concepts of Segmentation and Paging:5M Address Translation Mechanism:5M	10
C.	Perform the multiplication between -6 and 4 using the Booth's Algorithm for signed integer algorithm with the help of flowchart. Flowchart-4 M Calculation-6M	10
D.	Explain various operating modes of 8255 and its interfacing with 8086. Operating Modes-5 M for each mode(BSR &I/O)	10
E.	Draw and explain 4-stage pipeline to explain the concept of Instruction Pipelining. Also, specify features of Multicore processor Architecture. Features-4M Pipelining-6 M	10
Q.3	Attempt any FOUR. (All questions carry equal marks)	
A.	Draw and explain basic architecture of a computer system. Explanation 2M Diagram 3 M	05
B.	Consider a 2-way set associative mapped cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find- 1. Number of bits in tag(3M) 2. Tag directory size(2M) 4 Bits, 320 bits	05
C.	Draw and explain architecture of 8255 Peripheral Programmable Interface IC. 8255 Architecture-5 M	05
D.	Explain the pointer and index registers in 8086 with their functions. Pointer register-2.5M Index registers- 2.5M	05